CLAIMS

What is claimed is:

1. An adaptive analog equalizer that operates on an input signal and outputs an output signal, comprising:

a high pass network;

a multiplier, having an adjustable gain using gain control;

wherein said equalizer has a frequency response adapted to compensate for corruption in said input signal;

wherein said gain control uses said output signal to adjust said adjustable gain of said multiplier; and

wherein said equalizer modifies said input signal by summing said first input signal with itself.

2. The adaptive analog equalizer of claim 1, wherein said input signal comprises a channel corrupted input signal.

3. The adaptive analog equalizer of claim 1, wherein said input signal is provided from a communication channel, said communication channel having a channel frequency response; and

said frequency response of said high pass network and said multiplier being substantially an inverse of said channel frequency response.

4. The adaptive analog equalizer of claim 1, wherein said gain control performs decision and sampling control of said output signal; and

said gain control integrates an output signal from said decision and sampling control using an integrator.

5. The adaptive analog equalizer of claim 1, further comprising a variable gain amplifier, an integrator, and a peak detector; and

wherein said output signal is passed through said peak detector and said integrator to provide a control signal for said variable gain amplifier.

6. The adaptive analog equalizer of claim 1, wherein said adaptive analog equalizer performs double sampling of said input signal.

7. The adaptive analog equalizer of claim 1, wherein said adaptive analog equalizer waits a first predetermined period of time after detecting a pulse rising edge before sampling a first sample of said input signal; and

said adaptive analog equalizer waits a second predetermined period of time after detecting said pulse rising edge before sampling a second sample of said input signal.

8. A double sampling adaptive analog equalizer, comprising:

a gain control unit comprising a decision and sampling control circuit, said decision and sampling control circuit being operable to perform double sampling of an input signal; and

said gain control unit comprising a gain control processed feedback loop that forces said input signal to a predetermined value within a bit period after detecting a pulse rising edge.

9. The double sampling adaptive analog equalizer of claim 8, wherein said decision and sampling circuit waits a first predetermined period of time after detecting said pulse rising edge before sampling a first sample of said input signal.

10. The double sampling adaptive analog equalizer of claim 9, wherein said first predetermined period of time is less than a pulse period.

11. The double sampling adaptive analog equalizer of claim 8, wherein said decision and sampling circuit waits a second predetermined period of time after detecting said pulse rising edge before sampling a second sample of said input signal.

12. The double sampling adaptive analog equalizer of claim 11, wherein said second predetermined period of time is greater than a pulse period.

13. The double sampling adaptive analog equalizer of claim 8, wherein said predetermined value is zero.

14. The double sampling adaptive analog equalizer of claim 8, wherein said adaptive analog equalizer structure comprises a high pass network and a multiplier having an adjustable gain.

15. The double sampling adaptive analog equalizer of claim 14, wherein said input signal is provided from a communication channel, said communication channel having a channel frequency response; and

a frequency response of said high pass network and said multiplier is substantially an inverse of said channel frequency response.

16. A method to perform analog adaptive equalization, said method allowed comprising:

detecting a pulse rising edge of an input signal;

waiting a first predetermined period of time after detecting said pulse rising edge before sampling a first sample of said input signal;

waiting a second predetermined period of time after detecting said pulse rising edge before sampling a second sample of said input signal; and

adjusting a gain of a multiplier when said second sample does not exceed a predetermined threshold.

17. The method of claim 16, wherein said first predetermined period of time is less than a pulse period.

18. The method of claim 16, wherein said second predetermined period of time is greater than a pulse period.

19. The method of claim 16, wherein said input signal comprises a channel corrupted input signal.

20. The method of claim 16, further comprising forcing said input signal to zero within a bit period after detecting said pulse rising edge in response to a one to zero transition.